Laboratory Report

**Course:** Coen 316 **Lab Section:** DL-X

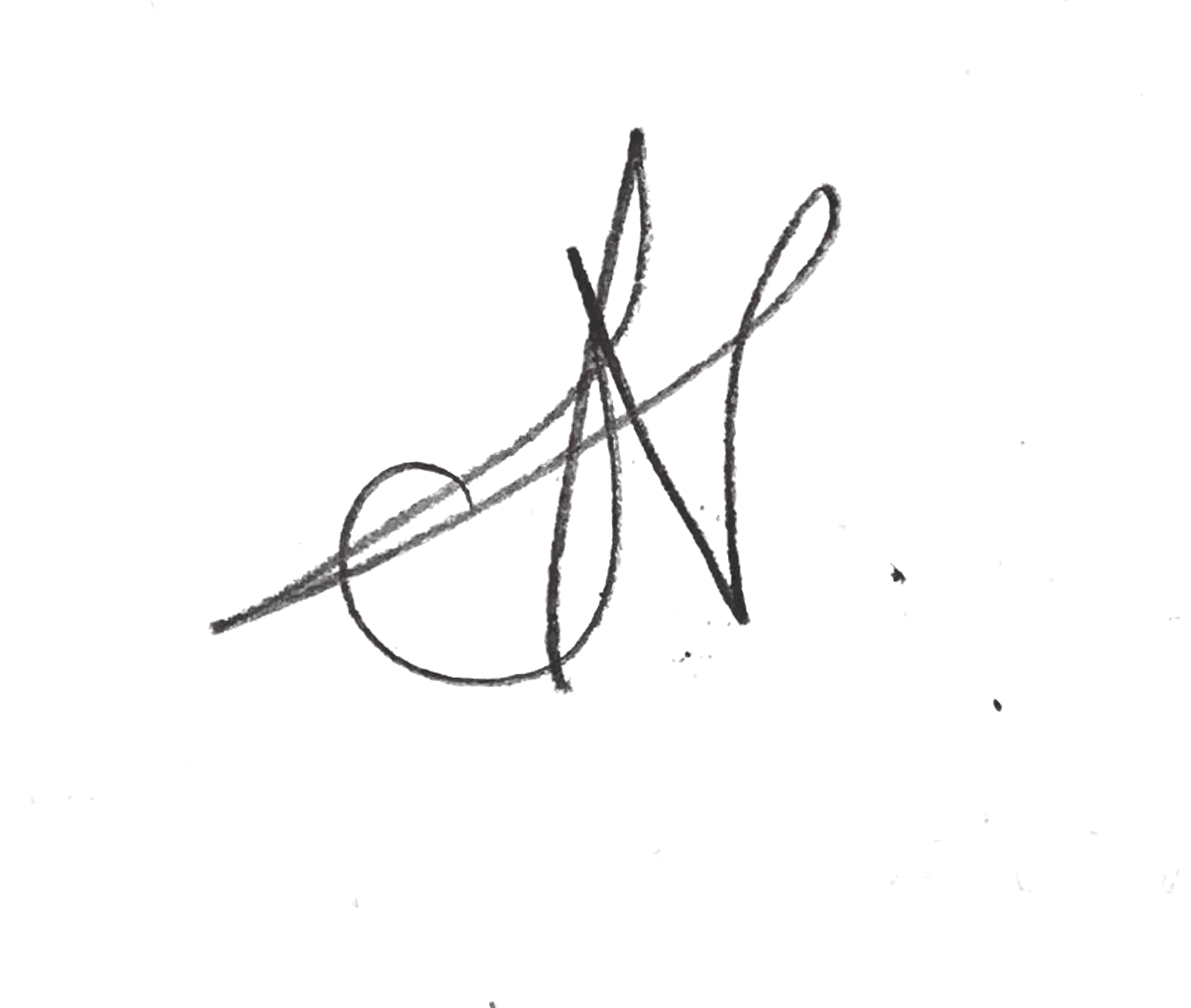
**Experiment No:** 2 **Date Performed:** 2023 – 10 – 05

**Report Due Date:** 2023 – 10 – 26

**Name:** Noah Louvet **ID:** 40086114

**I certify that this submission is my original work and meets the Faculty’s Expectations of Originality**

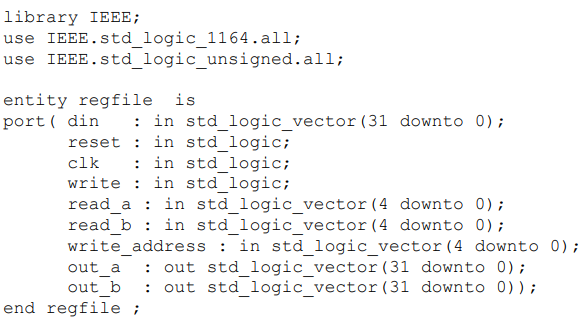
**Signature:**  **Date:** 2023 – 10 – 05



**Objectives**

The objective of this laboratory experiment is to design a multi-port register file in VHDL, adhering to the given entity specification. The register file should consist of 32 registers, each having 32 bits.

**Introduction**



***Figure 1***: Entity specification

A diagram of a computer code

Description automatically generated

***Figure 2***: Register file block diagram

Implement Read and Write Operations: Implement two read ports (out\_a and out\_b) which output the contents of specified registers based on the 5-bit addresses provided on read\_a and read\_b input ports. Ensure that reading happens asynchronously, independent of the clock input. Additionally, implement a write port that allows data (presented on the din input port) to be written into a specific register determined by the 5-bit address on the write\_address input. Writing should be synchronous, occurring at the rising edge of the clock signal and controlled by the active high write signal.

Reset Functionality: Incorporate a reset functionality where the entire register file can be cleared to 0 by asserting the asynchronous active-high reset input.

Input Validation: Ensure proper validation of input addresses (read\_a, read\_b, and write\_address) to prevent accessing registers beyond the specified 32 registers (R0-R31).

Timing and Control: Ensure that the read operations are asynchronous and independent of the clock signal. Write operations should be synchronized with the rising edge of the clock signal and controlled by the active high write signal.

**Results**

In this part I’ll be showing the results of the conducted lab with screenshots at every step.

**32-bit source code:**

A screenshot of a computer code

Description automatically generated

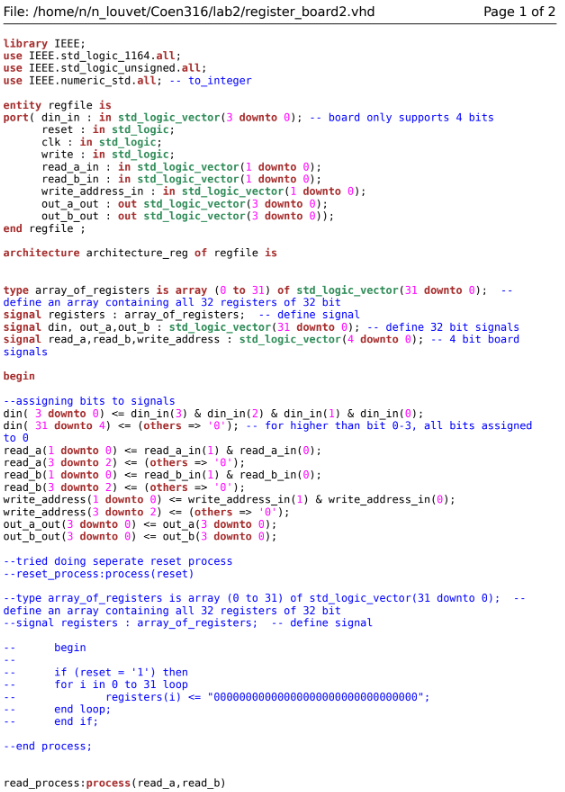
A screenshot of a computer code

Description automatically generated

A computer screen shot of a code

Description automatically generated

***Figure 3*:** register2.vhd

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**A computer screen shot of a code

Description automatically generated**

***Figure 4*:** Board wrapper (4-bit version)

**A screenshot of a computer code

Description automatically generated**

***Figure 5*:** Contraints file .xdc

**A screenshot of a computer

Description automatically generated**



***Figure 6*:** modelsim waveform

During simulation, I identified that it works properly except for the delayed update. It seems like the update happens when the next read or write process is processed. I have an idea how to solve this problem, do the update outside of the processes before the “end archicture\_reg”, however despite having an idea why this is happening I was not able to implement the adjustment. This would explain why I start the do file with a reset but until the run 2 is done and the next cycle starts the values are not zero but undefined. However we were able to validate the code despite the delayed update.

**A screenshot of a computer program

Description automatically generated**

**A screenshot of a computer program

Description automatically generated**

***Figure 7*:** DO file

Vivado logs can be found in the appendix section.

**Conclusion**

In conclusion, this lab focused on designing a 32 x 32 multi-port register file using VHDL. The register file featured two read ports, one write port with write enable, and the ability to reset all registers asynchronously. The design allowed for synchronous writing and asynchronous reading. The lab also required simulation using Modelsim, synthesis with Xilinx Vivado tools, and implementation on an FPGA board which were successfully provided.

**Appendix**

The logs contained some warnings due to the unused bits as the board can only accommodate for 4 bits, the synthesis and implementation as well as generation of the bistream were successful as these warnings can be neglected.

**Vivado Synthesis**

\*\*\* Running vivado

with args -log regfile.vds -m64 -product Vivado -mode batch -messageDb vivado.pb -notrace -source regfile.tcl

\*\*\*\*\*\* Vivado v2018.2 (64-bit)

\*\*\*\* SW Build 2258646 on Thu Jun 14 20:02:38 MDT 2018

\*\*\*\* IP Build 2256618 on Thu Jun 14 22:10:49 MDT 2018

\*\* Copyright 1986-2018 Xilinx, Inc. All Rights Reserved.

source regfile.tcl -notrace

Command: synth\_design -top regfile -part xc7a100tcsg324-1

Starting synth\_design

Attempting to get a license for feature 'Synthesis' and/or device 'xc7a100t'

INFO: [Common 17-349] Got license for feature 'Synthesis' and/or device 'xc7a100t'

INFO: Launching helper process for spawning children vivado processes

INFO: Helper process launched with PID 17294

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Starting RTL Elaboration : Time (s): cpu = 00:00:01 ; elapsed = 00:00:03 . Memory (MB): peak = 1401.578 ; gain = 85.805 ; free physical = 12164 ; free virtual = 23689

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INFO: [Synth 8-638] synthesizing module 'regfile' [/nfs/home/n/n\_louvet/Coen316/lab2/vivado/lab2\_316/lab2\_316.srcs/sources\_1/imports/lab2/register\_board2.vhd:18]

WARNING: [Synth 8-614] signal 'all\_32\_registers' is read in the process but is not in the sensitivity list [/nfs/home/n/n\_louvet/Coen316/lab2/vivado/lab2\_316/lab2\_316.srcs/sources\_1/imports/lab2/register\_board2.vhd:56]

WARNING: [Synth 8-3936] Found unconnected internal register 'out\_b\_reg' and it is trimmed from '32' to '4' bits. [/nfs/home/n/n\_louvet/Coen316/lab2/vivado/lab2\_316/lab2\_316.srcs/sources\_1/imports/lab2/register\_board2.vhd:38]

WARNING: [Synth 8-3936] Found unconnected internal register 'out\_a\_reg' and it is trimmed from '32' to '4' bits. [/nfs/home/n/n\_louvet/Coen316/lab2/vivado/lab2\_316/lab2\_316.srcs/sources\_1/imports/lab2/register\_board2.vhd:37]

INFO: [Synth 8-256] done synthesizing module 'regfile' (1#1) [/nfs/home/n/n\_louvet/Coen316/lab2/vivado/lab2\_316/lab2\_316.srcs/sources\_1/imports/lab2/register\_board2.vhd:18]

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Finished RTL Elaboration : Time (s): cpu = 00:00:02 ; elapsed = 00:00:05 . Memory (MB): peak = 1446.219 ; gain = 130.445 ; free physical = 12176 ; free virtual = 23703

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Report Check Netlist:

+------+------------------+-------+---------+-------+------------------+

| |Item |Errors |Warnings |Status |Description |

+------+------------------+-------+---------+-------+------------------+

|1 |multi\_driven\_nets | 0| 0|Passed |Multi driven nets |

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Start Handling Custom Attributes

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Finished Handling Custom Attributes : Time (s): cpu = 00:00:02 ; elapsed = 00:00:05 . Memory (MB): peak = 1446.219 ; gain = 130.445 ; free physical = 12176 ; free virtual = 23702

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Finished RTL Optimization Phase 1 : Time (s): cpu = 00:00:02 ; elapsed = 00:00:05 . Memory (MB): peak = 1446.219 ; gain = 130.445 ; free physical = 12176 ; free virtual = 23702

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INFO: [Device 21-403] Loading part xc7a100tcsg324-1

INFO: [Project 1-570] Preparing netlist for logic optimization

Processing XDC Constraints

Initializing timing engine

Parsing XDC File [/nfs/home/n/n\_louvet/Coen316/lab2/DO/register.xdc]

Finished Parsing XDC File [/nfs/home/n/n\_louvet/Coen316/lab2/DO/register.xdc]

INFO: [Project 1-236] Implementation specific constraints were found while reading constraint file [/nfs/home/n/n\_louvet/Coen316/lab2/DO/register.xdc]. These constraints will be ignored for synthesis but will be used in implementation. Impacted constraints are listed in the file [.Xil/regfile\_propImpl.xdc].

Resolution: To avoid this warning, move constraints listed in [.Xil/regfile\_propImpl.xdc] to another XDC file and exclude this new file from synthesis with the used\_in\_synthesis property (File Properties dialog in GUI) and re-run elaboration/synthesis.

Completed Processing XDC Constraints

INFO: [Project 1-111] Unisim Transformation Summary:

No Unisim elements were transformed.

Constraint Validation Runtime : Time (s): cpu = 00:00:00 ; elapsed = 00:00:00 . Memory (MB): peak = 1835.496 ; gain = 0.000 ; free physical = 11793 ; free virtual = 23352

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Finished Constraint Validation : Time (s): cpu = 00:00:10 ; elapsed = 00:00:42 . Memory (MB): peak = 1835.496 ; gain = 519.723 ; free physical = 11950 ; free virtual = 23508

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Start Loading Part and Timing Information

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Loading part: xc7a100tcsg324-1

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Finished Loading Part and Timing Information : Time (s): cpu = 00:00:10 ; elapsed = 00:00:42 . Memory (MB): peak = 1835.496 ; gain = 519.723 ; free physical = 11950 ; free virtual = 23508

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Start Applying 'set\_property' XDC Constraints

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Finished applying 'set\_property' XDC Constraints : Time (s): cpu = 00:00:10 ; elapsed = 00:00:42 . Memory (MB): peak = 1835.496 ; gain = 519.723 ; free physical = 11951 ; free virtual = 23510

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INFO: [Synth 8-5546] ROM "all\_32\_registers\_reg[0]" won't be mapped to RAM because it is too sparse

INFO: [Synth 8-5546] ROM "all\_32\_registers\_reg[1]" won't be mapped to RAM because it is too sparse

INFO: [Synth 8-5546] ROM "all\_32\_registers\_reg[2]" won't be mapped to RAM because it is too sparse

INFO: [Synth 8-5546] ROM "all\_32\_registers\_reg[3]" won't be mapped to RAM because it is too sparse

INFO: [Synth 8-5546] ROM "all\_32\_registers\_reg[4]" won't be mapped to RAM because it is too sparse

INFO: [Synth 8-5546] ROM "all\_32\_registers\_reg[5]" won't be mapped to RAM because it is too sparse

INFO: [Synth 8-5546] ROM "all\_32\_registers\_reg[6]" won't be mapped to RAM because it is too sparse

INFO: [Synth 8-5546] ROM "all\_32\_registers\_reg[7]" won't be mapped to RAM because it is too sparse

INFO: [Synth 8-5546] ROM "all\_32\_registers\_reg[8]" won't be mapped to RAM because it is too sparse

INFO: [Synth 8-5546] ROM "all\_32\_registers\_reg[9]" won't be mapped to RAM because it is too sparse

INFO: [Synth 8-5546] ROM "all\_32\_registers\_reg[10]" won't be mapped to RAM because it is too sparse

INFO: [Synth 8-5546] ROM "all\_32\_registers\_reg[11]" won't be mapped to RAM because it is too sparse

INFO: [Synth 8-5546] ROM "all\_32\_registers\_reg[12]" won't be mapped to RAM because it is too sparse

INFO: [Synth 8-5546] ROM "all\_32\_registers\_reg[13]" won't be mapped to RAM because it is too sparse

INFO: [Synth 8-5546] ROM "all\_32\_registers\_reg[14]" won't be mapped to RAM because it is too sparse

INFO: [Synth 8-5546] ROM "all\_32\_registers\_reg[15]" won't be mapped to RAM because it is too sparse

INFO: [Synth 8-5546] ROM "all\_32\_registers\_reg[16]" won't be mapped to RAM because it is too sparse

INFO: [Synth 8-5546] ROM "all\_32\_registers\_reg[17]" won't be mapped to RAM because it is too sparse

INFO: [Synth 8-5546] ROM "all\_32\_registers\_reg[18]" won't be mapped to RAM because it is too sparse

INFO: [Synth 8-5546] ROM "all\_32\_registers\_reg[19]" won't be mapped to RAM because it is too sparse

INFO: [Synth 8-5546] ROM "all\_32\_registers\_reg[20]" won't be mapped to RAM because it is too sparse

INFO: [Synth 8-5546] ROM "all\_32\_registers\_reg[21]" won't be mapped to RAM because it is too sparse

INFO: [Synth 8-5546] ROM "all\_32\_registers\_reg[22]" won't be mapped to RAM because it is too sparse

INFO: [Synth 8-5546] ROM "all\_32\_registers\_reg[23]" won't be mapped to RAM because it is too sparse

INFO: [Synth 8-5546] ROM "all\_32\_registers\_reg[24]" won't be mapped to RAM because it is too sparse

INFO: [Synth 8-5546] ROM "all\_32\_registers\_reg[25]" won't be mapped to RAM because it is too sparse

INFO: [Synth 8-5546] ROM "all\_32\_registers\_reg[26]" won't be mapped to RAM because it is too sparse

INFO: [Synth 8-5546] ROM "all\_32\_registers\_reg[27]" won't be mapped to RAM because it is too sparse

INFO: [Synth 8-5546] ROM "all\_32\_registers\_reg[28]" won't be mapped to RAM because it is too sparse

INFO: [Synth 8-5546] ROM "all\_32\_registers\_reg[29]" won't be mapped to RAM because it is too sparse

INFO: [Synth 8-5546] ROM "all\_32\_registers\_reg[30]" won't be mapped to RAM because it is too sparse

INFO: [Synth 8-5546] ROM "all\_32\_registers\_reg[31]" won't be mapped to RAM because it is too sparse

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Finished RTL Optimization Phase 2 : Time (s): cpu = 00:00:11 ; elapsed = 00:00:42 . Memory (MB): peak = 1835.496 ; gain = 519.723 ; free physical = 11935 ; free virtual = 23494

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Report RTL Partitions:

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| |RTL Partition |Replication |Instances |

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Start RTL Component Statistics

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Detailed RTL Component Info :

+---Registers :

32 Bit Registers := 32

+---Muxes :

32 Input 4 Bit Muxes := 2

2 Input 1 Bit Muxes := 8

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Finished RTL Component Statistics

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Start RTL Hierarchical Component Statistics

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Hierarchical RTL Component report

Module regfile

Detailed RTL Component Info :

+---Registers :

32 Bit Registers := 32

+---Muxes :

32 Input 4 Bit Muxes := 2

2 Input 1 Bit Muxes := 8

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Finished RTL Hierarchical Component Statistics

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Start Part Resource Summary

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Part Resources:

DSPs: 240 (col length:80)

BRAMs: 270 (col length: RAMB18 80 RAMB36 40)

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Finished Part Resource Summary

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Start Cross Boundary and Area Optimization

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Warning: Parallel synthesis criteria is not met

INFO: [Synth 8-4471] merging register 'all\_32\_registers\_reg[30][31:0]' into 'all\_32\_registers\_reg[31][31:0]' [/nfs/home/n/n\_louvet/Coen316/lab2/vivado/lab2\_316/lab2\_316.srcs/sources\_1/imports/lab2/register\_board2.vhd:72]

INFO: [Synth 8-4471] merging register 'all\_32\_registers\_reg[29][31:0]' into 'all\_32\_registers\_reg[31][31:0]' [/nfs/home/n/n\_louvet/Coen316/lab2/vivado/lab2\_316/lab2\_316.srcs/sources\_1/imports/lab2/register\_board2.vhd:72]

INFO: [Synth 8-4471] merging register 'all\_32\_registers\_reg[28][31:0]' into 'all\_32\_registers\_reg[31][31:0]' [/nfs/home/n/n\_louvet/Coen316/lab2/vivado/lab2\_316/lab2\_316.srcs/sources\_1/imports/lab2/register\_board2.vhd:72]

INFO: [Synth 8-4471] merging register 'all\_32\_registers\_reg[27][31:0]' into 'all\_32\_registers\_reg[31][31:0]' [/nfs/home/n/n\_louvet/Coen316/lab2/vivado/lab2\_316/lab2\_316.srcs/sources\_1/imports/lab2/register\_board2.vhd:72]

INFO: [Synth 8-4471] merging register 'all\_32\_registers\_reg[26][31:0]' into 'all\_32\_registers\_reg[31][31:0]' [/nfs/home/n/n\_louvet/Coen316/lab2/vivado/lab2\_316/lab2\_316.srcs/sources\_1/imports/lab2/register\_board2.vhd:72]

INFO: [Synth 8-4471] merging register 'all\_32\_registers\_reg[25][31:0]' into 'all\_32\_registers\_reg[31][31:0]' [/nfs/home/n/n\_louvet/Coen316/lab2/vivado/lab2\_316/lab2\_316.srcs/sources\_1/imports/lab2/register\_board2.vhd:72]

INFO: [Synth 8-4471] merging register 'all\_32\_registers\_reg[24][31:0]' into 'all\_32\_registers\_reg[31][31:0]' [/nfs/home/n/n\_louvet/Coen316/lab2/vivado/lab2\_316/lab2\_316.srcs/sources\_1/imports/lab2/register\_board2.vhd:72]

INFO: [Synth 8-4471] merging register 'all\_32\_registers\_reg[23][31:0]' into 'all\_32\_registers\_reg[31][31:0]' [/nfs/home/n/n\_louvet/Coen316/lab2/vivado/lab2\_316/lab2\_316.srcs/sources\_1/imports/lab2/register\_board2.vhd:72]

INFO: [Synth 8-4471] merging register 'all\_32\_registers\_reg[22][31:0]' into 'all\_32\_registers\_reg[31][31:0]' [/nfs/home/n/n\_louvet/Coen316/lab2/vivado/lab2\_316/lab2\_316.srcs/sources\_1/imports/lab2/register\_board2.vhd:72]

INFO: [Synth 8-4471] merging register 'all\_32\_registers\_reg[21][31:0]' into 'all\_32\_registers\_reg[31][31:0]' [/nfs/home/n/n\_louvet/Coen316/lab2/vivado/lab2\_316/lab2\_316.srcs/sources\_1/imports/lab2/register\_board2.vhd:72]

INFO: [Synth 8-4471] merging register 'all\_32\_registers\_reg[20][31:0]' into 'all\_32\_registers\_reg[31][31:0]' [/nfs/home/n/n\_louvet/Coen316/lab2/vivado/lab2\_316/lab2\_316.srcs/sources\_1/imports/lab2/register\_board2.vhd:72]

INFO: [Synth 8-4471] merging register 'all\_32\_registers\_reg[15][31:0]' into 'all\_32\_registers\_reg[31][31:0]' [/nfs/home/n/n\_louvet/Coen316/lab2/vivado/lab2\_316/lab2\_316.srcs/sources\_1/imports/lab2/register\_board2.vhd:72]

INFO: [Synth 8-4471] merging register 'all\_32\_registers\_reg[14][31:0]' into 'all\_32\_registers\_reg[31][31:0]' [/nfs/home/n/n\_louvet/Coen316/lab2/vivado/lab2\_316/lab2\_316.srcs/sources\_1/imports/lab2/register\_board2.vhd:72]

INFO: [Synth 8-4471] merging register 'all\_32\_registers\_reg[13][31:0]' into 'all\_32\_registers\_reg[31][31:0]' [/nfs/home/n/n\_louvet/Coen316/lab2/vivado/lab2\_316/lab2\_316.srcs/sources\_1/imports/lab2/register\_board2.vhd:72]

INFO: [Synth 8-4471] merging register 'all\_32\_registers\_reg[12][31:0]' into 'all\_32\_registers\_reg[31][31:0]' [/nfs/home/n/n\_louvet/Coen316/lab2/vivado/lab2\_316/lab2\_316.srcs/sources\_1/imports/lab2/register\_board2.vhd:72]

INFO: [Synth 8-4471] merging register 'all\_32\_registers\_reg[11][31:0]' into 'all\_32\_registers\_reg[31][31:0]' [/nfs/home/n/n\_louvet/Coen316/lab2/vivado/lab2\_316/lab2\_316.srcs/sources\_1/imports/lab2/register\_board2.vhd:72]

INFO: [Synth 8-4471] merging register 'all\_32\_registers\_reg[10][31:0]' into 'all\_32\_registers\_reg[31][31:0]' [/nfs/home/n/n\_louvet/Coen316/lab2/vivado/lab2\_316/lab2\_316.srcs/sources\_1/imports/lab2/register\_board2.vhd:72]

INFO: [Synth 8-4471] merging register 'all\_32\_registers\_reg[9][31:0]' into 'all\_32\_registers\_reg[31][31:0]' [/nfs/home/n/n\_louvet/Coen316/lab2/vivado/lab2\_316/lab2\_316.srcs/sources\_1/imports/lab2/register\_board2.vhd:72]

INFO: [Synth 8-4471] merging register 'all\_32\_registers\_reg[8][31:0]' into 'all\_32\_registers\_reg[31][31:0]' [/nfs/home/n/n\_louvet/Coen316/lab2/vivado/lab2\_316/lab2\_316.srcs/sources\_1/imports/lab2/register\_board2.vhd:72]

INFO: [Synth 8-4471] merging register 'all\_32\_registers\_reg[7][31:0]' into 'all\_32\_registers\_reg[31][31:0]' [/nfs/home/n/n\_louvet/Coen316/lab2/vivado/lab2\_316/lab2\_316.srcs/sources\_1/imports/lab2/register\_board2.vhd:72]

INFO: [Synth 8-4471] merging register 'all\_32\_registers\_reg[6][31:0]' into 'all\_32\_registers\_reg[31][31:0]' [/nfs/home/n/n\_louvet/Coen316/lab2/vivado/lab2\_316/lab2\_316.srcs/sources\_1/imports/lab2/register\_board2.vhd:72]

INFO: [Synth 8-4471] merging register 'all\_32\_registers\_reg[5][31:0]' into 'all\_32\_registers\_reg[31][31:0]' [/nfs/home/n/n\_louvet/Coen316/lab2/vivado/lab2\_316/lab2\_316.srcs/sources\_1/imports/lab2/register\_board2.vhd:72]

INFO: [Synth 8-4471] merging register 'all\_32\_registers\_reg[4][31:0]' into 'all\_32\_registers\_reg[31][31:0]' [/nfs/home/n/n\_louvet/Coen316/lab2/vivado/lab2\_316/lab2\_316.srcs/sources\_1/imports/lab2/register\_board2.vhd:72]

WARNING: [Synth 8-6014] Unused sequential element all\_32\_registers\_reg[30] was removed. [/nfs/home/n/n\_louvet/Coen316/lab2/vivado/lab2\_316/lab2\_316.srcs/sources\_1/imports/lab2/register\_board2.vhd:72]

WARNING: [Synth 8-6014] Unused sequential element all\_32\_registers\_reg[29] was removed. [/nfs/home/n/n\_louvet/Coen316/lab2/vivado/lab2\_316/lab2\_316.srcs/sources\_1/imports/lab2/register\_board2.vhd:72]

WARNING: [Synth 8-6014] Unused sequential element all\_32\_registers\_reg[28] was removed. [/nfs/home/n/n\_louvet/Coen316/lab2/vivado/lab2\_316/lab2\_316.srcs/sources\_1/imports/lab2/register\_board2.vhd:72]

WARNING: [Synth 8-6014] Unused sequential element all\_32\_registers\_reg[27] was removed. [/nfs/home/n/n\_louvet/Coen316/lab2/vivado/lab2\_316/lab2\_316.srcs/sources\_1/imports/lab2/register\_board2.vhd:72]

WARNING: [Synth 8-6014] Unused sequential element all\_32\_registers\_reg[26] was removed. [/nfs/home/n/n\_louvet/Coen316/lab2/vivado/lab2\_316/lab2\_316.srcs/sources\_1/imports/lab2/register\_board2.vhd:72]

WARNING: [Synth 8-6014] Unused sequential element all\_32\_registers\_reg[25] was removed. [/nfs/home/n/n\_louvet/Coen316/lab2/vivado/lab2\_316/lab2\_316.srcs/sources\_1/imports/lab2/register\_board2.vhd:72]

WARNING: [Synth 8-6014] Unused sequential element all\_32\_registers\_reg[24] was removed. [/nfs/home/n/n\_louvet/Coen316/lab2/vivado/lab2\_316/lab2\_316.srcs/sources\_1/imports/lab2/register\_board2.vhd:72]

WARNING: [Synth 8-6014] Unused sequential element all\_32\_registers\_reg[23] was removed. [/nfs/home/n/n\_louvet/Coen316/lab2/vivado/lab2\_316/lab2\_316.srcs/sources\_1/imports/lab2/register\_board2.vhd:72]

WARNING: [Synth 8-6014] Unused sequential element all\_32\_registers\_reg[22] was removed. [/nfs/home/n/n\_louvet/Coen316/lab2/vivado/lab2\_316/lab2\_316.srcs/sources\_1/imports/lab2/register\_board2.vhd:72]

WARNING: [Synth 8-6014] Unused sequential element all\_32\_registers\_reg[21] was removed. [/nfs/home/n/n\_louvet/Coen316/lab2/vivado/lab2\_316/lab2\_316.srcs/sources\_1/imports/lab2/register\_board2.vhd:72]

WARNING: [Synth 8-6014] Unused sequential element all\_32\_registers\_reg[20] was removed. [/nfs/home/n/n\_louvet/Coen316/lab2/vivado/lab2\_316/lab2\_316.srcs/sources\_1/imports/lab2/register\_board2.vhd:72]

WARNING: [Synth 8-6014] Unused sequential element all\_32\_registers\_reg[15] was removed. [/nfs/home/n/n\_louvet/Coen316/lab2/vivado/lab2\_316/lab2\_316.srcs/sources\_1/imports/lab2/register\_board2.vhd:72]

WARNING: [Synth 8-6014] Unused sequential element all\_32\_registers\_reg[14] was removed. [/nfs/home/n/n\_louvet/Coen316/lab2/vivado/lab2\_316/lab2\_316.srcs/sources\_1/imports/lab2/register\_board2.vhd:72]

WARNING: [Synth 8-6014] Unused sequential element all\_32\_registers\_reg[13] was removed. [/nfs/home/n/n\_louvet/Coen316/lab2/vivado/lab2\_316/lab2\_316.srcs/sources\_1/imports/lab2/register\_board2.vhd:72]

WARNING: [Synth 8-6014] Unused sequential element all\_32\_registers\_reg[12] was removed. [/nfs/home/n/n\_louvet/Coen316/lab2/vivado/lab2\_316/lab2\_316.srcs/sources\_1/imports/lab2/register\_board2.vhd:72]

WARNING: [Synth 8-6014] Unused sequential element all\_32\_registers\_reg[11] was removed. [/nfs/home/n/n\_louvet/Coen316/lab2/vivado/lab2\_316/lab2\_316.srcs/sources\_1/imports/lab2/register\_board2.vhd:72]

WARNING: [Synth 8-6014] Unused sequential element all\_32\_registers\_reg[10] was removed. [/nfs/home/n/n\_louvet/Coen316/lab2/vivado/lab2\_316/lab2\_316.srcs/sources\_1/imports/lab2/register\_board2.vhd:72]

WARNING: [Synth 8-6014] Unused sequential element all\_32\_registers\_reg[9] was removed. [/nfs/home/n/n\_louvet/Coen316/lab2/vivado/lab2\_316/lab2\_316.srcs/sources\_1/imports/lab2/register\_board2.vhd:72]

WARNING: [Synth 8-6014] Unused sequential element all\_32\_registers\_reg[8] was removed. [/nfs/home/n/n\_louvet/Coen316/lab2/vivado/lab2\_316/lab2\_316.srcs/sources\_1/imports/lab2/register\_board2.vhd:72]

WARNING: [Synth 8-6014] Unused sequential element all\_32\_registers\_reg[7] was removed. [/nfs/home/n/n\_louvet/Coen316/lab2/vivado/lab2\_316/lab2\_316.srcs/sources\_1/imports/lab2/register\_board2.vhd:72]

WARNING: [Synth 8-6014] Unused sequential element all\_32\_registers\_reg[6] was removed. [/nfs/home/n/n\_louvet/Coen316/lab2/vivado/lab2\_316/lab2\_316.srcs/sources\_1/imports/lab2/register\_board2.vhd:72]

WARNING: [Synth 8-6014] Unused sequential element all\_32\_registers\_reg[5] was removed. [/nfs/home/n/n\_louvet/Coen316/lab2/vivado/lab2\_316/lab2\_316.srcs/sources\_1/imports/lab2/register\_board2.vhd:72]

WARNING: [Synth 8-6014] Unused sequential element all\_32\_registers\_reg[4] was removed. [/nfs/home/n/n\_louvet/Coen316/lab2/vivado/lab2\_316/lab2\_316.srcs/sources\_1/imports/lab2/register\_board2.vhd:72]

INFO: [Synth 8-3886] merging instance 'all\_32\_registers\_reg[19][0]' (FDCE) to 'all\_32\_registers\_reg[17][0]'

INFO: [Synth 8-3886] merging instance 'all\_32\_registers\_reg[18][0]' (FDCE) to 'all\_32\_registers\_reg[17][0]'

INFO: [Synth 8-3886] merging instance 'all\_32\_registers\_reg[17][0]' (FDCE) to 'all\_32\_registers\_reg[31][0]'

INFO: [Synth 8-3886] merging instance 'all\_32\_registers\_reg[16][0]' (FDCE) to 'all\_32\_registers\_reg[31][0]'

INFO: [Synth 8-3333] propagating constant 0 across sequential element (\all\_32\_registers\_reg[31][0] )

INFO: [Synth 8-3886] merging instance 'all\_32\_registers\_reg[19][1]' (FDCE) to 'all\_32\_registers\_reg[17][1]'

INFO: [Synth 8-3886] merging instance 'all\_32\_registers\_reg[18][1]' (FDCE) to 'all\_32\_registers\_reg[17][1]'

INFO: [Synth 8-3886] merging instance 'all\_32\_registers\_reg[17][1]' (FDCE) to 'all\_32\_registers\_reg[31][1]'

INFO: [Synth 8-3886] merging instance 'all\_32\_registers\_reg[16][1]' (FDCE) to 'all\_32\_registers\_reg[31][1]'

INFO: [Synth 8-3333] propagating constant 0 across sequential element (\all\_32\_registers\_reg[31][1] )

INFO: [Synth 8-3886] merging instance 'all\_32\_registers\_reg[19][2]' (FDCE) to 'all\_32\_registers\_reg[17][2]'

INFO: [Synth 8-3886] merging instance 'all\_32\_registers\_reg[18][2]' (FDCE) to 'all\_32\_registers\_reg[17][2]'

INFO: [Synth 8-3886] merging instance 'all\_32\_registers\_reg[17][2]' (FDCE) to 'all\_32\_registers\_reg[31][2]'

INFO: [Synth 8-3886] merging instance 'all\_32\_registers\_reg[16][2]' (FDCE) to 'all\_32\_registers\_reg[31][2]'

INFO: [Synth 8-3333] propagating constant 0 across sequential element (\all\_32\_registers\_reg[31][2] )

INFO: [Synth 8-3886] merging instance 'all\_32\_registers\_reg[19][3]' (FDCE) to 'all\_32\_registers\_reg[17][3]'

INFO: [Synth 8-3886] merging instance 'all\_32\_registers\_reg[18][3]' (FDCE) to 'all\_32\_registers\_reg[17][3]'

INFO: [Synth 8-3886] merging instance 'all\_32\_registers\_reg[17][3]' (FDCE) to 'all\_32\_registers\_reg[31][3]'

INFO: [Synth 8-3886] merging instance 'all\_32\_registers\_reg[16][3]' (FDCE) to 'all\_32\_registers\_reg[31][3]'

INFO: [Synth 8-3333] propagating constant 0 across sequential element (\all\_32\_registers\_reg[31][3] )

WARNING: [Synth 8-3332] Sequential element (all\_32\_registers\_reg[31][31]) is unused and will be removed from module regfile.

WARNING: [Synth 8-3332] Sequential element (all\_32\_registers\_reg[31][30]) is unused and will be removed from module regfile.

WARNING: [Synth 8-3332] Sequential element (all\_32\_registers\_reg[31][29]) is unused and will be removed from module regfile.

WARNING: [Synth 8-3332] Sequential element (all\_32\_registers\_reg[31][28]) is unused and will be removed from module regfile.

WARNING: [Synth 8-3332] Sequential element (all\_32\_registers\_reg[31][27]) is unused and will be removed from module regfile.

WARNING: [Synth 8-3332] Sequential element (all\_32\_registers\_reg[31][26]) is unused and will be removed from module regfile.

WARNING: [Synth 8-3332] Sequential element (all\_32\_registers\_reg[31][25]) is unused and will be removed from module regfile.

WARNING: [Synth 8-3332] Sequential element (all\_32\_registers\_reg[31][24]) is unused and will be removed from module regfile.

WARNING: [Synth 8-3332] Sequential element (all\_32\_registers\_reg[31][23]) is unused and will be removed from module regfile.

WARNING: [Synth 8-3332] Sequential element (all\_32\_registers\_reg[31][22]) is unused and will be removed from module regfile.

WARNING: [Synth 8-3332] Sequential element (all\_32\_registers\_reg[31][21]) is unused and will be removed from module regfile.

WARNING: [Synth 8-3332] Sequential element (all\_32\_registers\_reg[31][20]) is unused and will be removed from module regfile.

WARNING: [Synth 8-3332] Sequential element (all\_32\_registers\_reg[31][19]) is unused and will be removed from module regfile.

WARNING: [Synth 8-3332] Sequential element (all\_32\_registers\_reg[31][18]) is unused and will be removed from module regfile.

WARNING: [Synth 8-3332] Sequential element (all\_32\_registers\_reg[31][17]) is unused and will be removed from module regfile.

WARNING: [Synth 8-3332] Sequential element (all\_32\_registers\_reg[31][16]) is unused and will be removed from module regfile.

WARNING: [Synth 8-3332] Sequential element (all\_32\_registers\_reg[31][15]) is unused and will be removed from module regfile.

WARNING: [Synth 8-3332] Sequential element (all\_32\_registers\_reg[31][14]) is unused and will be removed from module regfile.

WARNING: [Synth 8-3332] Sequential element (all\_32\_registers\_reg[31][13]) is unused and will be removed from module regfile.

WARNING: [Synth 8-3332] Sequential element (all\_32\_registers\_reg[31][12]) is unused and will be removed from module regfile.

WARNING: [Synth 8-3332] Sequential element (all\_32\_registers\_reg[31][11]) is unused and will be removed from module regfile.

WARNING: [Synth 8-3332] Sequential element (all\_32\_registers\_reg[31][10]) is unused and will be removed from module regfile.

WARNING: [Synth 8-3332] Sequential element (all\_32\_registers\_reg[31][9]) is unused and will be removed from module regfile.

WARNING: [Synth 8-3332] Sequential element (all\_32\_registers\_reg[31][8]) is unused and will be removed from module regfile.

WARNING: [Synth 8-3332] Sequential element (all\_32\_registers\_reg[31][7]) is unused and will be removed from module regfile.

WARNING: [Synth 8-3332] Sequential element (all\_32\_registers\_reg[31][6]) is unused and will be removed from module regfile.

WARNING: [Synth 8-3332] Sequential element (all\_32\_registers\_reg[31][5]) is unused and will be removed from module regfile.

WARNING: [Synth 8-3332] Sequential element (all\_32\_registers\_reg[31][4]) is unused and will be removed from module regfile.

WARNING: [Synth 8-3332] Sequential element (all\_32\_registers\_reg[19][31]) is unused and will be removed from module regfile.

WARNING: [Synth 8-3332] Sequential element (all\_32\_registers\_reg[19][30]) is unused and will be removed from module regfile.

WARNING: [Synth 8-3332] Sequential element (all\_32\_registers\_reg[19][29]) is unused and will be removed from module regfile.

WARNING: [Synth 8-3332] Sequential element (all\_32\_registers\_reg[19][28]) is unused and will be removed from module regfile.

WARNING: [Synth 8-3332] Sequential element (all\_32\_registers\_reg[19][27]) is unused and will be removed from module regfile.

WARNING: [Synth 8-3332] Sequential element (all\_32\_registers\_reg[19][26]) is unused and will be removed from module regfile.

WARNING: [Synth 8-3332] Sequential element (all\_32\_registers\_reg[19][25]) is unused and will be removed from module regfile.

WARNING: [Synth 8-3332] Sequential element (all\_32\_registers\_reg[19][24]) is unused and will be removed from module regfile.

WARNING: [Synth 8-3332] Sequential element (all\_32\_registers\_reg[19][23]) is unused and will be removed from module regfile.

WARNING: [Synth 8-3332] Sequential element (all\_32\_registers\_reg[19][22]) is unused and will be removed from module regfile.

WARNING: [Synth 8-3332] Sequential element (all\_32\_registers\_reg[19][21]) is unused and will be removed from module regfile.

WARNING: [Synth 8-3332] Sequential element (all\_32\_registers\_reg[19][20]) is unused and will be removed from module regfile.

WARNING: [Synth 8-3332] Sequential element (all\_32\_registers\_reg[19][19]) is unused and will be removed from module regfile.

WARNING: [Synth 8-3332] Sequential element (all\_32\_registers\_reg[19][18]) is unused and will be removed from module regfile.

WARNING: [Synth 8-3332] Sequential element (all\_32\_registers\_reg[19][17]) is unused and will be removed from module regfile.

WARNING: [Synth 8-3332] Sequential element (all\_32\_registers\_reg[19][16]) is unused and will be removed from module regfile.

WARNING: [Synth 8-3332] Sequential element (all\_32\_registers\_reg[19][15]) is unused and will be removed from module regfile.

WARNING: [Synth 8-3332] Sequential element (all\_32\_registers\_reg[19][14]) is unused and will be removed from module regfile.

WARNING: [Synth 8-3332] Sequential element (all\_32\_registers\_reg[19][13]) is unused and will be removed from module regfile.

WARNING: [Synth 8-3332] Sequential element (all\_32\_registers\_reg[19][12]) is unused and will be removed from module regfile.

WARNING: [Synth 8-3332] Sequential element (all\_32\_registers\_reg[19][11]) is unused and will be removed from module regfile.

WARNING: [Synth 8-3332] Sequential element (all\_32\_registers\_reg[19][10]) is unused and will be removed from module regfile.

WARNING: [Synth 8-3332] Sequential element (all\_32\_registers\_reg[19][9]) is unused and will be removed from module regfile.

WARNING: [Synth 8-3332] Sequential element (all\_32\_registers\_reg[19][8]) is unused and will be removed from module regfile.

WARNING: [Synth 8-3332] Sequential element (all\_32\_registers\_reg[19][7]) is unused and will be removed from module regfile.

WARNING: [Synth 8-3332] Sequential element (all\_32\_registers\_reg[19][6]) is unused and will be removed from module regfile.

WARNING: [Synth 8-3332] Sequential element (all\_32\_registers\_reg[19][5]) is unused and will be removed from module regfile.

WARNING: [Synth 8-3332] Sequential element (all\_32\_registers\_reg[19][4]) is unused and will be removed from module regfile.

WARNING: [Synth 8-3332] Sequential element (all\_32\_registers\_reg[18][31]) is unused and will be removed from module regfile.

WARNING: [Synth 8-3332] Sequential element (all\_32\_registers\_reg[18][30]) is unused and will be removed from module regfile.

WARNING: [Synth 8-3332] Sequential element (all\_32\_registers\_reg[18][29]) is unused and will be removed from module regfile.

WARNING: [Synth 8-3332] Sequential element (all\_32\_registers\_reg[18][28]) is unused and will be removed from module regfile.

WARNING: [Synth 8-3332] Sequential element (all\_32\_registers\_reg[18][27]) is unused and will be removed from module regfile.

WARNING: [Synth 8-3332] Sequential element (all\_32\_registers\_reg[18][26]) is unused and will be removed from module regfile.

WARNING: [Synth 8-3332] Sequential element (all\_32\_registers\_reg[18][25]) is unused and will be removed from module regfile.

WARNING: [Synth 8-3332] Sequential element (all\_32\_registers\_reg[18][24]) is unused and will be removed from module regfile.

WARNING: [Synth 8-3332] Sequential element (all\_32\_registers\_reg[18][23]) is unused and will be removed from module regfile.

WARNING: [Synth 8-3332] Sequential element (all\_32\_registers\_reg[18][22]) is unused and will be removed from module regfile.

WARNING: [Synth 8-3332] Sequential element (all\_32\_registers\_reg[18][21]) is unused and will be removed from module regfile.

WARNING: [Synth 8-3332] Sequential element (all\_32\_registers\_reg[18][20]) is unused and will be removed from module regfile.

WARNING: [Synth 8-3332] Sequential element (all\_32\_registers\_reg[18][19]) is unused and will be removed from module regfile.

WARNING: [Synth 8-3332] Sequential element (all\_32\_registers\_reg[18][18]) is unused and will be removed from module regfile.

WARNING: [Synth 8-3332] Sequential element (all\_32\_registers\_reg[18][17]) is unused and will be removed from module regfile.

WARNING: [Synth 8-3332] Sequential element (all\_32\_registers\_reg[18][16]) is unused and will be removed from module regfile.

WARNING: [Synth 8-3332] Sequential element (all\_32\_registers\_reg[18][15]) is unused and will be removed from module regfile.

WARNING: [Synth 8-3332] Sequential element (all\_32\_registers\_reg[18][14]) is unused and will be removed from module regfile.

WARNING: [Synth 8-3332] Sequential element (all\_32\_registers\_reg[18][13]) is unused and will be removed from module regfile.

WARNING: [Synth 8-3332] Sequential element (all\_32\_registers\_reg[18][12]) is unused and will be removed from module regfile.

WARNING: [Synth 8-3332] Sequential element (all\_32\_registers\_reg[18][11]) is unused and will be removed from module regfile.

WARNING: [Synth 8-3332] Sequential element (all\_32\_registers\_reg[18][10]) is unused and will be removed from module regfile.

WARNING: [Synth 8-3332] Sequential element (all\_32\_registers\_reg[18][9]) is unused and will be removed from module regfile.

WARNING: [Synth 8-3332] Sequential element (all\_32\_registers\_reg[18][8]) is unused and will be removed from module regfile.

WARNING: [Synth 8-3332] Sequential element (all\_32\_registers\_reg[18][7]) is unused and will be removed from module regfile.

WARNING: [Synth 8-3332] Sequential element (all\_32\_registers\_reg[18][6]) is unused and will be removed from module regfile.

WARNING: [Synth 8-3332] Sequential element (all\_32\_registers\_reg[18][5]) is unused and will be removed from module regfile.

WARNING: [Synth 8-3332] Sequential element (all\_32\_registers\_reg[18][4]) is unused and will be removed from module regfile.

WARNING: [Synth 8-3332] Sequential element (all\_32\_registers\_reg[17][31]) is unused and will be removed from module regfile.

WARNING: [Synth 8-3332] Sequential element (all\_32\_registers\_reg[17][30]) is unused and will be removed from module regfile.

WARNING: [Synth 8-3332] Sequential element (all\_32\_registers\_reg[17][29]) is unused and will be removed from module regfile.

WARNING: [Synth 8-3332] Sequential element (all\_32\_registers\_reg[17][28]) is unused and will be removed from module regfile.

WARNING: [Synth 8-3332] Sequential element (all\_32\_registers\_reg[17][27]) is unused and will be removed from module regfile.

WARNING: [Synth 8-3332] Sequential element (all\_32\_registers\_reg[17][26]) is unused and will be removed from module regfile.

WARNING: [Synth 8-3332] Sequential element (all\_32\_registers\_reg[17][25]) is unused and will be removed from module regfile.

WARNING: [Synth 8-3332] Sequential element (all\_32\_registers\_reg[17][24]) is unused and will be removed from module regfile.

WARNING: [Synth 8-3332] Sequential element (all\_32\_registers\_reg[17][23]) is unused and will be removed from module regfile.

WARNING: [Synth 8-3332] Sequential element (all\_32\_registers\_reg[17][22]) is unused and will be removed from module regfile.

WARNING: [Synth 8-3332] Sequential element (all\_32\_registers\_reg[17][21]) is unused and will be removed from module regfile.

WARNING: [Synth 8-3332] Sequential element (all\_32\_registers\_reg[17][20]) is unused and will be removed from module regfile.

WARNING: [Synth 8-3332] Sequential element (all\_32\_registers\_reg[17][19]) is unused and will be removed from module regfile.

WARNING: [Synth 8-3332] Sequential element (all\_32\_registers\_reg[17][18]) is unused and will be removed from module regfile.

WARNING: [Synth 8-3332] Sequential element (all\_32\_registers\_reg[17][17]) is unused and will be removed from module regfile.

WARNING: [Synth 8-3332] Sequential element (all\_32\_registers\_reg[17][16]) is unused and will be removed from module regfile.

INFO: [Common 17-14] Message 'Synth 8-3332' appears 100 times and further instances of the messages will be disabled. Use the Tcl command set\_msg\_config to change the current settings.

---------------------------------------------------------------------------------

Finished Cross Boundary and Area Optimization : Time (s): cpu = 00:00:11 ; elapsed = 00:00:43 . Memory (MB): peak = 1835.496 ; gain = 519.723 ; free physical = 11925 ; free virtual = 23485

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Report RTL Partitions:

+-+--------------+------------+----------+

| |RTL Partition |Replication |Instances |

+-+--------------+------------+----------+

+-+--------------+------------+----------+

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Start Applying XDC Timing Constraints

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Finished Applying XDC Timing Constraints : Time (s): cpu = 00:00:15 ; elapsed = 00:00:53 . Memory (MB): peak = 1835.496 ; gain = 519.723 ; free physical = 11807 ; free virtual = 23374

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---------------------------------------------------------------------------------

Start Timing Optimization

---------------------------------------------------------------------------------

---------------------------------------------------------------------------------

Finished Timing Optimization : Time (s): cpu = 00:00:15 ; elapsed = 00:00:53 . Memory (MB): peak = 1835.496 ; gain = 519.723 ; free physical = 11807 ; free virtual = 23374

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Report RTL Partitions:

+-+--------------+------------+----------+

| |RTL Partition |Replication |Instances |

+-+--------------+------------+----------+

+-+--------------+------------+----------+

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Start Technology Mapping

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Finished Technology Mapping : Time (s): cpu = 00:00:15 ; elapsed = 00:00:53 . Memory (MB): peak = 1835.496 ; gain = 519.723 ; free physical = 11806 ; free virtual = 23374

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Report RTL Partitions:

+-+--------------+------------+----------+

| |RTL Partition |Replication |Instances |

+-+--------------+------------+----------+

+-+--------------+------------+----------+

---------------------------------------------------------------------------------

Start IO Insertion

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---------------------------------------------------------------------------------

Start Flattening Before IO Insertion

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---------------------------------------------------------------------------------

Finished Flattening Before IO Insertion

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---------------------------------------------------------------------------------

Start Final Netlist Cleanup

---------------------------------------------------------------------------------

---------------------------------------------------------------------------------

Finished Final Netlist Cleanup

---------------------------------------------------------------------------------

---------------------------------------------------------------------------------

Finished IO Insertion : Time (s): cpu = 00:00:16 ; elapsed = 00:00:54 . Memory (MB): peak = 1835.496 ; gain = 519.723 ; free physical = 11806 ; free virtual = 23374

---------------------------------------------------------------------------------

Report Check Netlist:

+------+------------------+-------+---------+-------+------------------+

| |Item |Errors |Warnings |Status |Description |

+------+------------------+-------+---------+-------+------------------+

|1 |multi\_driven\_nets | 0| 0|Passed |Multi driven nets |

+------+------------------+-------+---------+-------+------------------+

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Start Renaming Generated Instances

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Finished Renaming Generated Instances : Time (s): cpu = 00:00:16 ; elapsed = 00:00:54 . Memory (MB): peak = 1835.496 ; gain = 519.723 ; free physical = 11806 ; free virtual = 23374

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Report RTL Partitions:

+-+--------------+------------+----------+

| |RTL Partition |Replication |Instances |

+-+--------------+------------+----------+

+-+--------------+------------+----------+

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Start Rebuilding User Hierarchy

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---------------------------------------------------------------------------------

Finished Rebuilding User Hierarchy : Time (s): cpu = 00:00:16 ; elapsed = 00:00:54 . Memory (MB): peak = 1835.496 ; gain = 519.723 ; free physical = 11806 ; free virtual = 23374

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Start Renaming Generated Ports

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Finished Renaming Generated Ports : Time (s): cpu = 00:00:16 ; elapsed = 00:00:54 . Memory (MB): peak = 1835.496 ; gain = 519.723 ; free physical = 11806 ; free virtual = 23374

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---------------------------------------------------------------------------------

Start Handling Custom Attributes

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---------------------------------------------------------------------------------

Finished Handling Custom Attributes : Time (s): cpu = 00:00:16 ; elapsed = 00:00:54 . Memory (MB): peak = 1835.496 ; gain = 519.723 ; free physical = 11806 ; free virtual = 23374

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Start Renaming Generated Nets

---------------------------------------------------------------------------------

---------------------------------------------------------------------------------

Finished Renaming Generated Nets : Time (s): cpu = 00:00:16 ; elapsed = 00:00:54 . Memory (MB): peak = 1835.496 ; gain = 519.723 ; free physical = 11806 ; free virtual = 23374

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Start Writing Synthesis Report

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Report BlackBoxes:

+-+--------------+----------+

| |BlackBox name |Instances |

+-+--------------+----------+

+-+--------------+----------+

Report Cell Usage:

+------+-----+------+

| |Cell |Count |

+------+-----+------+

|1 |BUFG | 1|

|2 |LUT3 | 4|

|3 |LUT6 | 8|

|4 |FDCE | 16|

|5 |IBUF | 13|

|6 |OBUF | 8|

+------+-----+------+

Report Instance Areas:

+------+---------+-------+------+

| |Instance |Module |Cells |

+------+---------+-------+------+

|1 |top | | 50|

+------+---------+-------+------+

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Finished Writing Synthesis Report : Time (s): cpu = 00:00:16 ; elapsed = 00:00:54 . Memory (MB): peak = 1835.496 ; gain = 519.723 ; free physical = 11806 ; free virtual = 23374

---------------------------------------------------------------------------------

Synthesis finished with 0 errors, 0 critical warnings and 279 warnings.

Synthesis Optimization Runtime : Time (s): cpu = 00:00:09 ; elapsed = 00:00:20 . Memory (MB): peak = 1835.496 ; gain = 130.445 ; free physical = 11860 ; free virtual = 23427

Synthesis Optimization Complete : Time (s): cpu = 00:00:16 ; elapsed = 00:00:54 . Memory (MB): peak = 1835.496 ; gain = 519.723 ; free physical = 11871 ; free virtual = 23438

INFO: [Project 1-571] Translating synthesized netlist

INFO: [Netlist 29-17] Analyzing 13 Unisim elements for replacement

INFO: [Netlist 29-28] Unisim Transformation completed in 0 CPU seconds

INFO: [Project 1-570] Preparing netlist for logic optimization

INFO: [Opt 31-138] Pushed 0 inverter(s) to 0 load pin(s).

INFO: [Project 1-111] Unisim Transformation Summary:

No Unisim elements were transformed.

INFO: [Common 17-83] Releasing license: Synthesis

90 Infos, 126 Warnings, 0 Critical Warnings and 0 Errors encountered.

synth\_design completed successfully

synth\_design: Time (s): cpu = 00:00:17 ; elapsed = 00:00:55 . Memory (MB): peak = 1835.496 ; gain = 532.371 ; free physical = 11854 ; free virtual = 23422

WARNING: [Constraints 18-5210] No constraint will be written out.

INFO: [Common 17-1381] The checkpoint '/nfs/home/n/n\_louvet/Coen316/lab2/vivado/lab2\_316/lab2\_316.runs/synth\_1/regfile.dcp' has been generated.

INFO: [runtcl-4] Executing : report\_utilization -file regfile\_utilization\_synth.rpt -pb regfile\_utilization\_synth.pb

report\_utilization: Time (s): cpu = 00:00:00.05 ; elapsed = 00:00:00.09 . Memory (MB): peak = 1835.496 ; gain = 0.000 ; free physical = 11855 ; free virtual = 23423

INFO: [Common 17-206] Exiting Vivado at Sat Oct 7 19:22:25 2023...

**Vivado Implementation**

\*\*\* Running vivado

with args -log regfile.vdi -applog -m64 -product Vivado -messageDb vivado.pb -mode batch -source regfile.tcl -notrace

\*\*\*\*\*\* Vivado v2018.2 (64-bit)

\*\*\*\* SW Build 2258646 on Thu Jun 14 20:02:38 MDT 2018

\*\*\*\* IP Build 2256618 on Thu Jun 14 22:10:49 MDT 2018

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source regfile.tcl -notrace

Command: link\_design -top regfile -part xc7a100tcsg324-1

Design is defaulting to srcset: sources\_1

Design is defaulting to constrset: constrs\_1

INFO: [Netlist 29-17] Analyzing 13 Unisim elements for replacement

INFO: [Netlist 29-28] Unisim Transformation completed in 0 CPU seconds

INFO: [Project 1-479] Netlist was created with Vivado 2018.2

INFO: [Device 21-403] Loading part xc7a100tcsg324-1

INFO: [Project 1-570] Preparing netlist for logic optimization

Parsing XDC File [/nfs/home/n/n\_louvet/Coen316/lab2/DO/register.xdc]

Finished Parsing XDC File [/nfs/home/n/n\_louvet/Coen316/lab2/DO/register.xdc]

INFO: [Opt 31-138] Pushed 0 inverter(s) to 0 load pin(s).

INFO: [Project 1-111] Unisim Transformation Summary:

No Unisim elements were transformed.

7 Infos, 0 Warnings, 0 Critical Warnings and 0 Errors encountered.

link\_design completed successfully

link\_design: Time (s): cpu = 00:00:07 ; elapsed = 00:00:30 . Memory (MB): peak = 1596.355 ; gain = 288.215 ; free physical = 11954 ; free virtual = 23520

Command: opt\_design

Attempting to get a license for feature 'Implementation' and/or device 'xc7a100t'

INFO: [Common 17-349] Got license for feature 'Implementation' and/or device 'xc7a100t'

Running DRC as a precondition to command opt\_design

Starting DRC Task

INFO: [DRC 23-27] Running DRC with 8 threads

INFO: [Project 1-461] DRC finished with 0 Errors

INFO: [Project 1-462] Please refer to the DRC report (report\_drc) for more information.

Time (s): cpu = 00:00:01 ; elapsed = 00:00:03 . Memory (MB): peak = 1689.383 ; gain = 93.027 ; free physical = 11948 ; free virtual = 23515

Starting Cache Timing Information Task

INFO: [Timing 38-35] Done setting XDC timing constraints.

Ending Cache Timing Information Task | Checksum: 95a23c3b

Time (s): cpu = 00:00:10 ; elapsed = 00:00:39 . Memory (MB): peak = 2134.883 ; gain = 445.500 ; free physical = 11473 ; free virtual = 23060

Starting Logic Optimization Task

Phase 1 Retarget

INFO: [Opt 31-138] Pushed 0 inverter(s) to 0 load pin(s).

INFO: [Opt 31-49] Retargeted 0 cell(s).

Phase 1 Retarget | Checksum: 95a23c3b

Time (s): cpu = 00:00:00.01 ; elapsed = 00:00:00.02 . Memory (MB): peak = 2134.883 ; gain = 0.000 ; free physical = 11548 ; free virtual = 23135

INFO: [Opt 31-389] Phase Retarget created 0 cells and removed 0 cells

Phase 2 Constant propagation

INFO: [Opt 31-138] Pushed 0 inverter(s) to 0 load pin(s).

Phase 2 Constant propagation | Checksum: 95a23c3b

Time (s): cpu = 00:00:00.01 ; elapsed = 00:00:00.02 . Memory (MB): peak = 2134.883 ; gain = 0.000 ; free physical = 11548 ; free virtual = 23135

INFO: [Opt 31-389] Phase Constant propagation created 0 cells and removed 0 cells

Phase 3 Sweep

Phase 3 Sweep | Checksum: 95a23c3b

Time (s): cpu = 00:00:00.01 ; elapsed = 00:00:00.02 . Memory (MB): peak = 2134.883 ; gain = 0.000 ; free physical = 11548 ; free virtual = 23135

INFO: [Opt 31-389] Phase Sweep created 0 cells and removed 0 cells

Phase 4 BUFG optimization

Phase 4 BUFG optimization | Checksum: 95a23c3b

Time (s): cpu = 00:00:00.02 ; elapsed = 00:00:00.02 . Memory (MB): peak = 2134.883 ; gain = 0.000 ; free physical = 11548 ; free virtual = 23135

INFO: [Opt 31-662] Phase BUFG optimization created 0 cells of which 0 are BUFGs and removed 0 cells.

Phase 5 Shift Register Optimization

Phase 5 Shift Register Optimization | Checksum: 95a23c3b

Time (s): cpu = 00:00:00.02 ; elapsed = 00:00:00.02 . Memory (MB): peak = 2134.883 ; gain = 0.000 ; free physical = 11548 ; free virtual = 23135

INFO: [Opt 31-389] Phase Shift Register Optimization created 0 cells and removed 0 cells

Phase 6 Post Processing Netlist

Phase 6 Post Processing Netlist | Checksum: 95a23c3b

Time (s): cpu = 00:00:00.02 ; elapsed = 00:00:00.02 . Memory (MB): peak = 2134.883 ; gain = 0.000 ; free physical = 11548 ; free virtual = 23135

INFO: [Opt 31-389] Phase Post Processing Netlist created 0 cells and removed 0 cells

Starting Connectivity Check Task

Time (s): cpu = 00:00:00 ; elapsed = 00:00:00 . Memory (MB): peak = 2134.883 ; gain = 0.000 ; free physical = 11548 ; free virtual = 23135

Ending Logic Optimization Task | Checksum: 95a23c3b

Time (s): cpu = 00:00:00.02 ; elapsed = 00:00:00.02 . Memory (MB): peak = 2134.883 ; gain = 0.000 ; free physical = 11548 ; free virtual = 23135

Starting Power Optimization Task

INFO: [Pwropt 34-132] Skipping clock gating for clocks with a period < 2.00 ns.

Ending Power Optimization Task | Checksum: 95a23c3b

Time (s): cpu = 00:00:00.01 ; elapsed = 00:00:00.03 . Memory (MB): peak = 2134.883 ; gain = 0.000 ; free physical = 11548 ; free virtual = 23135

Starting Final Cleanup Task

Ending Final Cleanup Task | Checksum: 95a23c3b

Time (s): cpu = 00:00:00 ; elapsed = 00:00:00 . Memory (MB): peak = 2134.883 ; gain = 0.000 ; free physical = 11548 ; free virtual = 23135

INFO: [Common 17-83] Releasing license: Implementation

23 Infos, 0 Warnings, 0 Critical Warnings and 0 Errors encountered.

opt\_design completed successfully

opt\_design: Time (s): cpu = 00:00:11 ; elapsed = 00:00:41 . Memory (MB): peak = 2134.883 ; gain = 538.527 ; free physical = 11548 ; free virtual = 23135

INFO: [Timing 38-480] Writing timing data to binary archive.

Writing placer database...

Writing XDEF routing.

Writing XDEF routing logical nets.

Writing XDEF routing special nets.

Write XDEF Complete: Time (s): cpu = 00:00:00.04 ; elapsed = 00:00:00.10 . Memory (MB): peak = 2166.898 ; gain = 0.004 ; free physical = 11545 ; free virtual = 23133

INFO: [Common 17-1381] The checkpoint '/nfs/home/n/n\_louvet/Coen316/lab2/vivado/lab2\_316/lab2\_316.runs/impl\_1/regfile\_opt.dcp' has been generated.

INFO: [runtcl-4] Executing : report\_drc -file regfile\_drc\_opted.rpt -pb regfile\_drc\_opted.pb -rpx regfile\_drc\_opted.rpx

Command: report\_drc -file regfile\_drc\_opted.rpt -pb regfile\_drc\_opted.pb -rpx regfile\_drc\_opted.rpx

INFO: [IP\_Flow 19-234] Refreshing IP repositories

INFO: [IP\_Flow 19-1704] No user IP repositories specified

INFO: [IP\_Flow 19-2313] Loaded Vivado IP repository '/CMC/tools/xilinx/Vivado\_2018.2/Vivado/2018.2/data/ip'.

INFO: [DRC 23-27] Running DRC with 8 threads

INFO: [Coretcl 2-168] The results of DRC are in file /nfs/home/n/n\_louvet/Coen316/lab2/vivado/lab2\_316/lab2\_316.runs/impl\_1/regfile\_drc\_opted.rpt.

report\_drc completed successfully

report\_drc: Time (s): cpu = 00:00:03 ; elapsed = 00:00:05 . Memory (MB): peak = 2246.938 ; gain = 80.031 ; free physical = 11505 ; free virtual = 23093

Command: place\_design

Attempting to get a license for feature 'Implementation' and/or device 'xc7a100t'

INFO: [Common 17-349] Got license for feature 'Implementation' and/or device 'xc7a100t'

INFO: [DRC 23-27] Running DRC with 8 threads

INFO: [Vivado\_Tcl 4-198] DRC finished with 0 Errors

INFO: [Vivado\_Tcl 4-199] Please refer to the DRC report (report\_drc) for more information.

Running DRC as a precondition to command place\_design

INFO: [DRC 23-27] Running DRC with 8 threads

INFO: [Vivado\_Tcl 4-198] DRC finished with 0 Errors

INFO: [Vivado\_Tcl 4-199] Please refer to the DRC report (report\_drc) for more information.

Starting Placer Task

INFO: [Place 30-611] Multithreading enabled for place\_design using a maximum of 8 CPUs

Phase 1 Placer Initialization

Phase 1.1 Placer Initialization Netlist Sorting

Netlist sorting complete. Time (s): cpu = 00:00:00 ; elapsed = 00:00:00 . Memory (MB): peak = 2246.938 ; gain = 0.000 ; free physical = 11502 ; free virtual = 23089

Phase 1.1 Placer Initialization Netlist Sorting | Checksum: 73a65b50

Time (s): cpu = 00:00:00 ; elapsed = 00:00:00.02 . Memory (MB): peak = 2246.938 ; gain = 0.000 ; free physical = 11502 ; free virtual = 23089

Netlist sorting complete. Time (s): cpu = 00:00:00 ; elapsed = 00:00:00 . Memory (MB): peak = 2246.938 ; gain = 0.000 ; free physical = 11502 ; free virtual = 23089

Phase 1.2 IO Placement/ Clock Placement/ Build Placer Device

INFO: [Timing 38-35] Done setting XDC timing constraints.

WARNING: [Place 30-574] Poor placement for routing between an IO pin and BUFG. This is normally an ERROR but the CLOCK\_DEDICATED\_ROUTE constraint is set to FALSE allowing your design to continue. The use of this override is highly discouraged as it may lead to very poor timing results. It is recommended that this error condition be corrected in the design.

clk\_IBUF\_inst (IBUF.O) is locked to IOB\_X0Y58

clk\_IBUF\_BUFG\_inst (BUFG.I) is provisionally placed by clockplacer on BUFGCTRL\_X0Y0

Resolution: Poor placement of an IO pin and a BUFG has resulted in the router using a non-dedicated path between the two. There are several things that could trigger this DRC, each of which can cause unpredictable clock insertion delays that result in poor timing. This DRC could be caused by any of the following: (a) a clock port was placed on a pin that is not a CCIO-pin (b)the BUFG has not been placed in the same half of the device or SLR as the CCIO-pin (c) a single ended clock has been placed on the N-Side of a differential pair CCIO-pin.

Phase 1.2 IO Placement/ Clock Placement/ Build Placer Device | Checksum: 2a1652cd

Time (s): cpu = 00:00:00.89 ; elapsed = 00:00:00.44 . Memory (MB): peak = 2246.938 ; gain = 0.000 ; free physical = 11501 ; free virtual = 23090

Phase 1.3 Build Placer Netlist Model

Phase 1.3 Build Placer Netlist Model | Checksum: f53a3e4b

Time (s): cpu = 00:00:00.95 ; elapsed = 00:00:00.46 . Memory (MB): peak = 2246.938 ; gain = 0.000 ; free physical = 11503 ; free virtual = 23092

Phase 1.4 Constrain Clocks/Macros

Phase 1.4 Constrain Clocks/Macros | Checksum: f53a3e4b

Time (s): cpu = 00:00:00.95 ; elapsed = 00:00:00.46 . Memory (MB): peak = 2246.938 ; gain = 0.000 ; free physical = 11503 ; free virtual = 23092

Phase 1 Placer Initialization | Checksum: f53a3e4b

Time (s): cpu = 00:00:00.96 ; elapsed = 00:00:00.46 . Memory (MB): peak = 2246.938 ; gain = 0.000 ; free physical = 11503 ; free virtual = 23092

Phase 2 Global Placement

Phase 2.1 Floorplanning

Phase 2.1 Floorplanning | Checksum: f53a3e4b

Time (s): cpu = 00:00:00.99 ; elapsed = 00:00:00.48 . Memory (MB): peak = 2246.938 ; gain = 0.000 ; free physical = 11502 ; free virtual = 23091

WARNING: [Place 46-29] place\_design is not in timing mode. Skip physical synthesis in placer

Phase 2 Global Placement | Checksum: ef7db015

Time (s): cpu = 00:00:02 ; elapsed = 00:00:00.62 . Memory (MB): peak = 2362.984 ; gain = 116.047 ; free physical = 11481 ; free virtual = 23070

Phase 3 Detail Placement

Phase 3.1 Commit Multi Column Macros

Phase 3.1 Commit Multi Column Macros | Checksum: ef7db015

Time (s): cpu = 00:00:02 ; elapsed = 00:00:00.62 . Memory (MB): peak = 2362.984 ; gain = 116.047 ; free physical = 11481 ; free virtual = 23070

Phase 3.2 Commit Most Macros & LUTRAMs

Phase 3.2 Commit Most Macros & LUTRAMs | Checksum: 8f0172c1

Time (s): cpu = 00:00:02 ; elapsed = 00:00:00.64 . Memory (MB): peak = 2362.984 ; gain = 116.047 ; free physical = 11480 ; free virtual = 23069

Phase 3.3 Area Swap Optimization

Phase 3.3 Area Swap Optimization | Checksum: adf07935

Time (s): cpu = 00:00:02 ; elapsed = 00:00:00.65 . Memory (MB): peak = 2362.984 ; gain = 116.047 ; free physical = 11480 ; free virtual = 23069

Phase 3.4 Pipeline Register Optimization

Phase 3.4 Pipeline Register Optimization | Checksum: adf07935

Time (s): cpu = 00:00:02 ; elapsed = 00:00:00.65 . Memory (MB): peak = 2362.984 ; gain = 116.047 ; free physical = 11480 ; free virtual = 23069

Phase 3.5 Small Shape Detail Placement

Phase 3.5 Small Shape Detail Placement | Checksum: 12c6548e4

Time (s): cpu = 00:00:02 ; elapsed = 00:00:00.74 . Memory (MB): peak = 2362.984 ; gain = 116.047 ; free physical = 11478 ; free virtual = 23067

Phase 3.6 Re-assign LUT pins

Phase 3.6 Re-assign LUT pins | Checksum: 12c6548e4

Time (s): cpu = 00:00:02 ; elapsed = 00:00:00.74 . Memory (MB): peak = 2362.984 ; gain = 116.047 ; free physical = 11478 ; free virtual = 23067

Phase 3.7 Pipeline Register Optimization

Phase 3.7 Pipeline Register Optimization | Checksum: 12c6548e4

Time (s): cpu = 00:00:02 ; elapsed = 00:00:00.74 . Memory (MB): peak = 2362.984 ; gain = 116.047 ; free physical = 11478 ; free virtual = 23067

Phase 3 Detail Placement | Checksum: 12c6548e4

Time (s): cpu = 00:00:02 ; elapsed = 00:00:00.75 . Memory (MB): peak = 2362.984 ; gain = 116.047 ; free physical = 11478 ; free virtual = 23067

Phase 4 Post Placement Optimization and Clean-Up

Phase 4.1 Post Commit Optimization

Phase 4.1 Post Commit Optimization | Checksum: 12c6548e4

Time (s): cpu = 00:00:02 ; elapsed = 00:00:00.75 . Memory (MB): peak = 2362.984 ; gain = 116.047 ; free physical = 11478 ; free virtual = 23067

Phase 4.2 Post Placement Cleanup

Phase 4.2 Post Placement Cleanup | Checksum: 12c6548e4

Time (s): cpu = 00:00:02 ; elapsed = 00:00:00.75 . Memory (MB): peak = 2362.984 ; gain = 116.047 ; free physical = 11480 ; free virtual = 23069

Phase 4.3 Placer Reporting

Phase 4.3 Placer Reporting | Checksum: 12c6548e4

Time (s): cpu = 00:00:02 ; elapsed = 00:00:00.75 . Memory (MB): peak = 2362.984 ; gain = 116.047 ; free physical = 11480 ; free virtual = 23069

Phase 4.4 Final Placement Cleanup

Phase 4.4 Final Placement Cleanup | Checksum: 12c6548e4

Time (s): cpu = 00:00:02 ; elapsed = 00:00:00.75 . Memory (MB): peak = 2362.984 ; gain = 116.047 ; free physical = 11480 ; free virtual = 23069

Phase 4 Post Placement Optimization and Clean-Up | Checksum: 12c6548e4

Time (s): cpu = 00:00:02 ; elapsed = 00:00:00.75 . Memory (MB): peak = 2362.984 ; gain = 116.047 ; free physical = 11480 ; free virtual = 23069

Ending Placer Task | Checksum: 8bc72357

Time (s): cpu = 00:00:02 ; elapsed = 00:00:00.76 . Memory (MB): peak = 2362.984 ; gain = 116.047 ; free physical = 11497 ; free virtual = 23086

INFO: [Common 17-83] Releasing license: Implementation

41 Infos, 2 Warnings, 0 Critical Warnings and 0 Errors encountered.

place\_design completed successfully

INFO: [Timing 38-480] Writing timing data to binary archive.

Writing placer database...

Writing XDEF routing.

Writing XDEF routing logical nets.

Writing XDEF routing special nets.

Write XDEF Complete: Time (s): cpu = 00:00:00.04 ; elapsed = 00:00:00.11 . Memory (MB): peak = 2362.984 ; gain = 0.000 ; free physical = 11496 ; free virtual = 23086

INFO: [Common 17-1381] The checkpoint '/nfs/home/n/n\_louvet/Coen316/lab2/vivado/lab2\_316/lab2\_316.runs/impl\_1/regfile\_placed.dcp' has been generated.

INFO: [runtcl-4] Executing : report\_io -file regfile\_io\_placed.rpt

report\_io: Time (s): cpu = 00:00:00.05 ; elapsed = 00:00:00.10 . Memory (MB): peak = 2362.984 ; gain = 0.000 ; free physical = 11490 ; free virtual = 23079

INFO: [runtcl-4] Executing : report\_utilization -file regfile\_utilization\_placed.rpt -pb regfile\_utilization\_placed.pb

report\_utilization: Time (s): cpu = 00:00:00.04 ; elapsed = 00:00:00.06 . Memory (MB): peak = 2362.984 ; gain = 0.000 ; free physical = 11497 ; free virtual = 23086

INFO: [runtcl-4] Executing : report\_control\_sets -verbose -file regfile\_control\_sets\_placed.rpt

report\_control\_sets: Time (s): cpu = 00:00:00 ; elapsed = 00:00:00.04 . Memory (MB): peak = 2362.984 ; gain = 0.000 ; free physical = 11496 ; free virtual = 23085

Command: route\_design

Attempting to get a license for feature 'Implementation' and/or device 'xc7a100t'

INFO: [Common 17-349] Got license for feature 'Implementation' and/or device 'xc7a100t'

Running DRC as a precondition to command route\_design

INFO: [DRC 23-27] Running DRC with 8 threads

WARNING: [DRC PLCK-12] Clock Placer Checks: Poor placement for routing between an IO pin and BUFG.

Resolution: Poor placement of an IO pin and a BUFG has resulted in the router using a non-dedicated path between the two. There are several things that could trigger this DRC, each of which can cause unpredictable clock insertion delays that result in poor timing. This DRC could be caused by any of the following: (a) a clock port was placed on a pin that is not a CCIO-pin (b)the BUFG has not been placed in the same half of the device or SLR as the CCIO-pin (c) a single ended clock has been placed on the N-Side of a differential pair CCIO-pin.

This is normally an ERROR but the CLOCK\_DEDICATED\_ROUTE constraint is set to FALSE allowing your design to continue. The use of this override is highly discouraged as it may lead to very poor timing results. It is recommended that this error condition be corrected in the design.

clk\_IBUF\_inst (IBUF.O) is locked to IOB\_X0Y58

clk\_IBUF\_BUFG\_inst (BUFG.I) is provisionally placed by clockplacer on BUFGCTRL\_X0Y0

INFO: [Vivado\_Tcl 4-198] DRC finished with 0 Errors, 1 Warnings

INFO: [Vivado\_Tcl 4-199] Please refer to the DRC report (report\_drc) for more information.

Starting Routing Task

INFO: [Route 35-254] Multithreading enabled for route\_design using a maximum of 8 CPUs

Checksum: PlaceDB: 64277bae ConstDB: 0 ShapeSum: 279fa7a9 RouteDB: 0

Phase 1 Build RT Design

Phase 1 Build RT Design | Checksum: ec47a83a

Time (s): cpu = 00:00:16 ; elapsed = 00:00:13 . Memory (MB): peak = 2399.984 ; gain = 37.000 ; free physical = 11343 ; free virtual = 22932

Post Restoration Checksum: NetGraph: 9f792b7 NumContArr: e2501583 Constraints: 0 Timing: 0

Phase 2 Router Initialization

INFO: [Route 35-64] No timing constraints were detected. The router will operate in resource-optimization mode.

Phase 2.1 Fix Topology Constraints

Phase 2.1 Fix Topology Constraints | Checksum: ec47a83a

Time (s): cpu = 00:00:16 ; elapsed = 00:00:13 . Memory (MB): peak = 2406.973 ; gain = 43.988 ; free physical = 11312 ; free virtual = 22901

Phase 2.2 Pre Route Cleanup

Phase 2.2 Pre Route Cleanup | Checksum: ec47a83a

Time (s): cpu = 00:00:16 ; elapsed = 00:00:13 . Memory (MB): peak = 2406.973 ; gain = 43.988 ; free physical = 11312 ; free virtual = 22901

Number of Nodes with overlaps = 0

Phase 2 Router Initialization | Checksum: 11712c582

Time (s): cpu = 00:00:16 ; elapsed = 00:00:13 . Memory (MB): peak = 2417.238 ; gain = 54.254 ; free physical = 11303 ; free virtual = 22892

Phase 3 Initial Routing

Phase 3 Initial Routing | Checksum: 10570f13f

Time (s): cpu = 00:00:16 ; elapsed = 00:00:13 . Memory (MB): peak = 2417.238 ; gain = 54.254 ; free physical = 11307 ; free virtual = 22896

Phase 4 Rip-up And Reroute

Phase 4.1 Global Iteration 0

Number of Nodes with overlaps = 2

Number of Nodes with overlaps = 0

Phase 4.1 Global Iteration 0 | Checksum: e29f720b

Time (s): cpu = 00:00:17 ; elapsed = 00:00:13 . Memory (MB): peak = 2417.238 ; gain = 54.254 ; free physical = 11307 ; free virtual = 22896

Phase 4 Rip-up And Reroute | Checksum: e29f720b

Time (s): cpu = 00:00:17 ; elapsed = 00:00:13 . Memory (MB): peak = 2417.238 ; gain = 54.254 ; free physical = 11307 ; free virtual = 22896

Phase 5 Delay and Skew Optimization

Phase 5 Delay and Skew Optimization | Checksum: e29f720b

Time (s): cpu = 00:00:17 ; elapsed = 00:00:13 . Memory (MB): peak = 2417.238 ; gain = 54.254 ; free physical = 11307 ; free virtual = 22896

Phase 6 Post Hold Fix

Phase 6.1 Hold Fix Iter

Phase 6.1 Hold Fix Iter | Checksum: e29f720b

Time (s): cpu = 00:00:17 ; elapsed = 00:00:13 . Memory (MB): peak = 2417.238 ; gain = 54.254 ; free physical = 11307 ; free virtual = 22896

Phase 6 Post Hold Fix | Checksum: e29f720b

Time (s): cpu = 00:00:17 ; elapsed = 00:00:13 . Memory (MB): peak = 2417.238 ; gain = 54.254 ; free physical = 11307 ; free virtual = 22896

Phase 7 Route finalize

Router Utilization Summary

Global Vertical Routing Utilization = 0.0184097 %

Global Horizontal Routing Utilization = 0.0125746 %

Routable Net Status\*

\*Does not include unroutable nets such as driverless and loadless.

Run report\_route\_status for detailed report.

Number of Failed Nets = 0

Number of Unrouted Nets = 0

Number of Partially Routed Nets = 0

Number of Node Overlaps = 0

Congestion Report

North Dir 1x1 Area, Max Cong = 19.8198%, No Congested Regions.

South Dir 1x1 Area, Max Cong = 21.6216%, No Congested Regions.

East Dir 1x1 Area, Max Cong = 5.88235%, No Congested Regions.

West Dir 1x1 Area, Max Cong = 7.35294%, No Congested Regions.

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Reporting congestion hotspots

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Direction: North

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Congested clusters found at Level 0

Effective congestion level: 0 Aspect Ratio: 1 Sparse Ratio: 0

Direction: South

----------------

Congested clusters found at Level 0

Effective congestion level: 0 Aspect Ratio: 1 Sparse Ratio: 0

Direction: East

----------------

Congested clusters found at Level 0

Effective congestion level: 0 Aspect Ratio: 1 Sparse Ratio: 0

Direction: West

----------------

Congested clusters found at Level 0

Effective congestion level: 0 Aspect Ratio: 1 Sparse Ratio: 0

Phase 7 Route finalize | Checksum: e29f720b

Time (s): cpu = 00:00:17 ; elapsed = 00:00:13 . Memory (MB): peak = 2417.238 ; gain = 54.254 ; free physical = 11307 ; free virtual = 22896

Phase 8 Verifying routed nets

Verification completed successfully

Phase 8 Verifying routed nets | Checksum: e29f720b

Time (s): cpu = 00:00:17 ; elapsed = 00:00:13 . Memory (MB): peak = 2419.238 ; gain = 56.254 ; free physical = 11306 ; free virtual = 22895

Phase 9 Depositing Routes

Phase 9 Depositing Routes | Checksum: da3c92bb

Time (s): cpu = 00:00:17 ; elapsed = 00:00:13 . Memory (MB): peak = 2419.238 ; gain = 56.254 ; free physical = 11306 ; free virtual = 22895

INFO: [Route 35-16] Router Completed Successfully

Time (s): cpu = 00:00:17 ; elapsed = 00:00:13 . Memory (MB): peak = 2419.238 ; gain = 56.254 ; free physical = 11341 ; free virtual = 22930

Routing Is Done.

INFO: [Common 17-83] Releasing license: Implementation

54 Infos, 3 Warnings, 0 Critical Warnings and 0 Errors encountered.

route\_design completed successfully

route\_design: Time (s): cpu = 00:00:18 ; elapsed = 00:00:15 . Memory (MB): peak = 2419.242 ; gain = 56.258 ; free physical = 11341 ; free virtual = 22930

INFO: [Timing 38-480] Writing timing data to binary archive.

Writing placer database...

Writing XDEF routing.

Writing XDEF routing logical nets.

Writing XDEF routing special nets.

Write XDEF Complete: Time (s): cpu = 00:00:00.10 ; elapsed = 00:00:00.12 . Memory (MB): peak = 2419.242 ; gain = 0.000 ; free physical = 11338 ; free virtual = 22928

INFO: [Common 17-1381] The checkpoint '/nfs/home/n/n\_louvet/Coen316/lab2/vivado/lab2\_316/lab2\_316.runs/impl\_1/regfile\_routed.dcp' has been generated.

INFO: [runtcl-4] Executing : report\_drc -file regfile\_drc\_routed.rpt -pb regfile\_drc\_routed.pb -rpx regfile\_drc\_routed.rpx

Command: report\_drc -file regfile\_drc\_routed.rpt -pb regfile\_drc\_routed.pb -rpx regfile\_drc\_routed.rpx

INFO: [DRC 23-27] Running DRC with 8 threads

INFO: [Coretcl 2-168] The results of DRC are in file /nfs/home/n/n\_louvet/Coen316/lab2/vivado/lab2\_316/lab2\_316.runs/impl\_1/regfile\_drc\_routed.rpt.

report\_drc completed successfully

INFO: [runtcl-4] Executing : report\_methodology -file regfile\_methodology\_drc\_routed.rpt -pb regfile\_methodology\_drc\_routed.pb -rpx regfile\_methodology\_drc\_routed.rpx

Command: report\_methodology -file regfile\_methodology\_drc\_routed.rpt -pb regfile\_methodology\_drc\_routed.pb -rpx regfile\_methodology\_drc\_routed.rpx

INFO: [Timing 38-35] Done setting XDC timing constraints.

INFO: [Timing 38-35] Done setting XDC timing constraints.

INFO: [DRC 23-133] Running Methodology with 8 threads

INFO: [Coretcl 2-1520] The results of Report Methodology are in file /nfs/home/n/n\_louvet/Coen316/lab2/vivado/lab2\_316/lab2\_316.runs/impl\_1/regfile\_methodology\_drc\_routed.rpt.

report\_methodology completed successfully

INFO: [runtcl-4] Executing : report\_power -file regfile\_power\_routed.rpt -pb regfile\_power\_summary\_routed.pb -rpx regfile\_power\_routed.rpx

Command: report\_power -file regfile\_power\_routed.rpt -pb regfile\_power\_summary\_routed.pb -rpx regfile\_power\_routed.rpx

WARNING: [Power 33-232] No user defined clocks were found in the design!

Resolution: Please specify clocks using create\_clock/create\_generated\_clock for sequential elements. For pure combinatorial circuits, please specify a virtual clock, otherwise the vectorless estimation might be inaccurate

INFO: [Timing 38-35] Done setting XDC timing constraints.

Running Vector-less Activity Propagation...

Finished Running Vector-less Activity Propagation

66 Infos, 4 Warnings, 0 Critical Warnings and 0 Errors encountered.

report\_power completed successfully

INFO: [runtcl-4] Executing : report\_route\_status -file regfile\_route\_status.rpt -pb regfile\_route\_status.pb

INFO: [runtcl-4] Executing : report\_timing\_summary -max\_paths 10 -file regfile\_timing\_summary\_routed.rpt -pb regfile\_timing\_summary\_routed.pb -rpx regfile\_timing\_summary\_routed.rpx -warn\_on\_violation

INFO: [Timing 38-91] UpdateTimingParams: Speed grade: -1, Delay Type: min\_max, Timing Stage: Requireds.

INFO: [Timing 38-191] Multithreading enabled for timing update using a maximum of 8 CPUs

WARNING: [Timing 38-313] There are no user specified timing constraints. Timing constraints are needed for proper timing analysis.

INFO: [runtcl-4] Executing : report\_incremental\_reuse -file regfile\_incremental\_reuse\_routed.rpt

INFO: [Vivado\_Tcl 4-545] No incremental reuse to report, no incremental placement and routing data was found.

INFO: [runtcl-4] Executing : report\_clock\_utilization -file regfile\_clock\_utilization\_routed.rpt

INFO: [runtcl-4] Executing : report\_bus\_skew -warn\_on\_violation -file regfile\_bus\_skew\_routed.rpt -pb regfile\_bus\_skew\_routed.pb -rpx regfile\_bus\_skew\_routed.rpx

INFO: [Timing 38-91] UpdateTimingParams: Speed grade: -1, Delay Type: min\_max, Timing Stage: Requireds.

INFO: [Timing 38-191] Multithreading enabled for timing update using a maximum of 8 CPUs

INFO: [Common 17-206] Exiting Vivado at Sat Oct 7 19:24:28 2023...

\*\*\* Running vivado

with args -log regfile.vdi -applog -m64 -product Vivado -messageDb vivado.pb -mode batch -source regfile.tcl -notrace

\*\*\*\*\*\* Vivado v2018.2 (64-bit)

\*\*\*\* SW Build 2258646 on Thu Jun 14 20:02:38 MDT 2018

\*\*\*\* IP Build 2256618 on Thu Jun 14 22:10:49 MDT 2018

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source regfile.tcl -notrace

Command: open\_checkpoint regfile\_routed.dcp

Starting open\_checkpoint Task

Time (s): cpu = 00:00:00.04 ; elapsed = 00:00:00.12 . Memory (MB): peak = 1277.121 ; gain = 0.000 ; free physical = 12252 ; free virtual = 23841

INFO: [Netlist 29-17] Analyzing 13 Unisim elements for replacement

INFO: [Netlist 29-28] Unisim Transformation completed in 0 CPU seconds

INFO: [Project 1-479] Netlist was created with Vivado 2018.2

INFO: [Device 21-403] Loading part xc7a100tcsg324-1

INFO: [Project 1-570] Preparing netlist for logic optimization

INFO: [Timing 38-478] Restoring timing data from binary archive.

INFO: [Timing 38-479] Binary timing data restore complete.

INFO: [Project 1-856] Restoring constraints from binary archive.

INFO: [Project 1-853] Binary constraint restore complete.

Reading XDEF placement.

Reading placer database...

Reading XDEF routing.

Read XDEF File: Time (s): cpu = 00:00:00.08 ; elapsed = 00:00:00.22 . Memory (MB): peak = 2087.070 ; gain = 0.004 ; free physical = 11519 ; free virtual = 23109

Restored from archive | CPU: 0.210000 secs | Memory: 0.983368 MB |

Finished XDEF File Restore: Time (s): cpu = 00:00:00.08 ; elapsed = 00:00:00.22 . Memory (MB): peak = 2087.070 ; gain = 0.004 ; free physical = 11519 ; free virtual = 23109

INFO: [Project 1-111] Unisim Transformation Summary:

No Unisim elements were transformed.

INFO: [Project 1-604] Checkpoint was created with Vivado v2018.2 (64-bit) build 2258646

open\_checkpoint: Time (s): cpu = 00:00:17 ; elapsed = 00:01:08 . Memory (MB): peak = 2087.070 ; gain = 809.953 ; free physical = 11519 ; free virtual = 23109

Command: write\_bitstream -force regfile.bit

Attempting to get a license for feature 'Implementation' and/or device 'xc7a100t'

INFO: [Common 17-349] Got license for feature 'Implementation' and/or device 'xc7a100t'

Running DRC as a precondition to command write\_bitstream

INFO: [IP\_Flow 19-234] Refreshing IP repositories

INFO: [IP\_Flow 19-1704] No user IP repositories specified

INFO: [IP\_Flow 19-2313] Loaded Vivado IP repository '/CMC/tools/xilinx/Vivado\_2018.2/Vivado/2018.2/data/ip'.

INFO: [DRC 23-27] Running DRC with 8 threads

WARNING: [DRC CFGBVS-1] Missing CFGBVS and CONFIG\_VOLTAGE Design Properties: Neither the CFGBVS nor CONFIG\_VOLTAGE voltage property is set in the current\_design. Configuration bank voltage select (CFGBVS) must be set to VCCO or GND, and CONFIG\_VOLTAGE must be set to the correct configuration voltage, in order to determine the I/O voltage support for the pins in bank 0. It is suggested to specify these either using the 'Edit Device Properties' function in the GUI or directly in the XDC file using the following syntax:

set\_property CFGBVS value1 [current\_design]

#where value1 is either VCCO or GND

set\_property CONFIG\_VOLTAGE value2 [current\_design]

#where value2 is the voltage provided to configuration bank 0

Refer to the device configuration user guide for more information.

INFO: [Vivado 12-3199] DRC finished with 0 Errors, 1 Warnings

INFO: [Vivado 12-3200] Please refer to the DRC report (report\_drc) for more information.

INFO: [Designutils 20-2272] Running write\_bitstream with 8 threads.

Loading data files...

Loading site data...

Loading route data...

Processing options...

Creating bitmap...

Creating bitstream...

Writing bitstream ./regfile.bit...

INFO: [Vivado 12-1842] Bitgen Completed Successfully.

INFO: [Common 17-83] Releasing license: Implementation

21 Infos, 1 Warnings, 0 Critical Warnings and 0 Errors encountered.

write\_bitstream completed successfully

write\_bitstream: Time (s): cpu = 00:00:08 ; elapsed = 00:00:12 . Memory (MB): peak = 2558.910 ; gain = 471.840 ; free physical = 11448 ; free virtual = 23046

INFO: [Common 17-206] Exiting Vivado at Sat Oct 7 19:26:16 2023...